

PLC Input Configuration Value

Revised: 091808

Value	I0	I1	I2	I3	I4	I5	I6	I7
default 0	TTL Input 0	TTL Output 1	Opto D1 Input	Opto D2 Input	GPIO Control Bit 1	GPIO Control Bit 0	Pulse Generator 1 out	Pulse Generator 0 out
1	CL FVAL	CL LVAL	GPIO Control Bit 3	GPIO Control Bit 2	CL DVAL	CL Spare	Rescaler 0 out	Pulse Generator 2 out
2	TTL Input 1	TTL Input 0	TTL Input 0	TTL Input 0	TTL Input 0	TTL Inout 0	TTL Input 0	TTL Input 0
3	LVDS Input	Opto Input	TTL Input 1	TTL Input 1	TTL Input1	TTL Inout 1	TTL Input 1	TTL Input 1
4	CL LVAL	CL FVAL	CL FVAL	Reserved	LVDS Input	Opto Input	Reserved	Opto Input
5	CL DVAL	CL Spare	Reserved	Reserved	Reserved	CL LVAL	Reserved	CL FVAL
6	GPIO Control Bit 0	GPIO Control Bit 0	Reserved	Reserved	CL LVAL	Reserved	Reserved	CL LVAL
7	GPIO Control Bit 1	GPIO Control Bit 1	GPIO Control Bit 0	GPIO Control Bit 0	Timestamp Trigger 3	Timestamp Trigger 2	CL DVAL	CL Spare
8	GPIO Control Bit 2	GPIO Control Bit 2	GPIO Control Bit 1	GPIO Control Bit 1	GPIO Control Bit 2	GPIO Control Bit 3	Timestamp Trigger 1	GPIO Control Bit 0
9	Q2 (feedback)	Q4 (feedback)	Q2 (feedback)	Q3 (feedback)	Q2 (feedback)	Q3 (feedback)	GPIO Control Bit 1	GPIO Control Bit 1
10	CC3 (feedback)	CC4 (feedback)	CC3 (feedback)	CC4 (feedback)	CC3 (feedback)	CC4 (feedback)	GPIO Control Bit 2	Timestamp Trigger 0
11	Pulse Generator 0 out	Pulse Generator 2 out	Pulse Generator 0 out	Pulse Generator 2 out	Pulse Generator 0 out	Pulse Generator 2 out	Q2 (feedback)	Q3 (feedback)
12	Pulse Generator 1 out	Pulse Generator 3 out	Pulse Generator 1 out	Pulse Generator 3 out	Reserved	Reserved	CC3 (feedback)	CC4 (feedback)
13	Rescaler 0 out	Rescaler 0 out	Rescaler 0 out	Rescaler 0 out	Rescaler 0 out	Rescaler 0 out	Pulse Generator 3 out	Reserved
14	Reserved	Reserved	Delayer 0 out	Delayer 0 out	Delayer 0 out	Delayer 0 out	Delayer 0 out	Reserved
15	Reserved	Reserved	Counter 0 Equal	Counter 0 Greater	Counter 0 Equal	Counter 0 Greater	Counter 0 Equal	Counter 0 Greater

GEViCAM Output Connections allocated to Specific Signals

Output	Functional Description	GPIO Connector Pin	Default	Signal in GEV
Q0	Connected to Internal Trigger Input (VINIT)	9	I0 (TTL Input)	A0 - A3
Q1	Connected to External Strobe output	3	I1 (TTL Output)	PLC_A4 = FVAL
Q2		5+, 11-	I2 (Opto D1 input)	PLC_A5 = LVAL
Q3	Connected to Optoisolated Output D2; Interrupt, Clear input (default)	6+, 12-	Q3 (Opto D2 output)	PLC_A6
Q4				
Q5				
Q6				
Q7	Interrupt, Clear input			
Q8	Pulse Generator 1 Trigger Input, Clear input			
Q9	Pulse Generator 0 Trigger Input, Clear input			
Q10	Pulse generator 3 Trigger Input; Interrupt, Clear input			
Q11	Pulse Generator 2 Trigger Input			
Q12				
Q13				
Q14	Grabber Trigger			
Q15	Interrupt (default)			
Q16	Clear input			
Q17	Clear input, Up Count			

The diagram illustrates the internal architecture of the PLC BLOCK. It shows a central LUT (Logic User Table) block that receives inputs from various sources and produces outputs. The inputs include:

- GPIO Connector:** Ext. Trigger (#9), Strobe Pulse Internal, Opto D1-IN (pins 5, 11), Opto D2-IN* (pins 6, 12), RS-485 (pins 4, 10), Audio IN (pin 14), and Audio OUT (pin 13).
- IO Block (Inputs):** TTL_IN0, TTL_IN1, Opto_IN2, and Opto_IN3.
- LUT:** Receives signals from the IO blocks and outputs to Q0, Q1, Q2, and Q3.
- IO Block (Outputs):** TTL_OUT0, TTL_OUT1, Opto_OUT2, and Opto_OUT3.
- GPIO Connector (Outputs):** Internal Trigger (#9), Strobe/Monitor OUT (#3), Opto D1-OUT* (pins 5, 11), Opto D2-OUT (pins 6, 12), RS485 Transceiver (pins 4, 10), and Audio CODEC (pins 14, 13).

GPIO Connector Pins 1, 2 and 7 are GND.